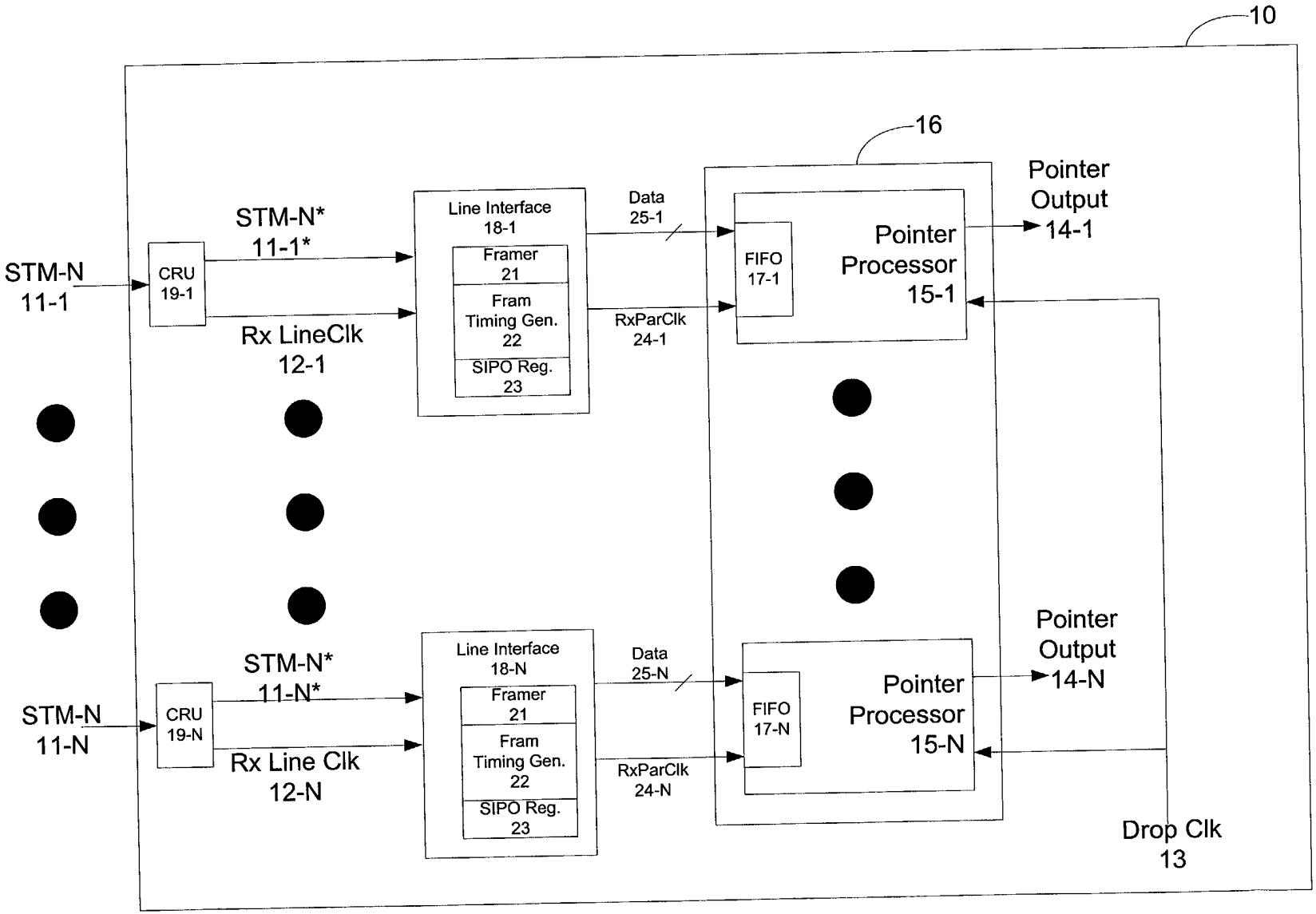

Figure 1 (Prior Art)

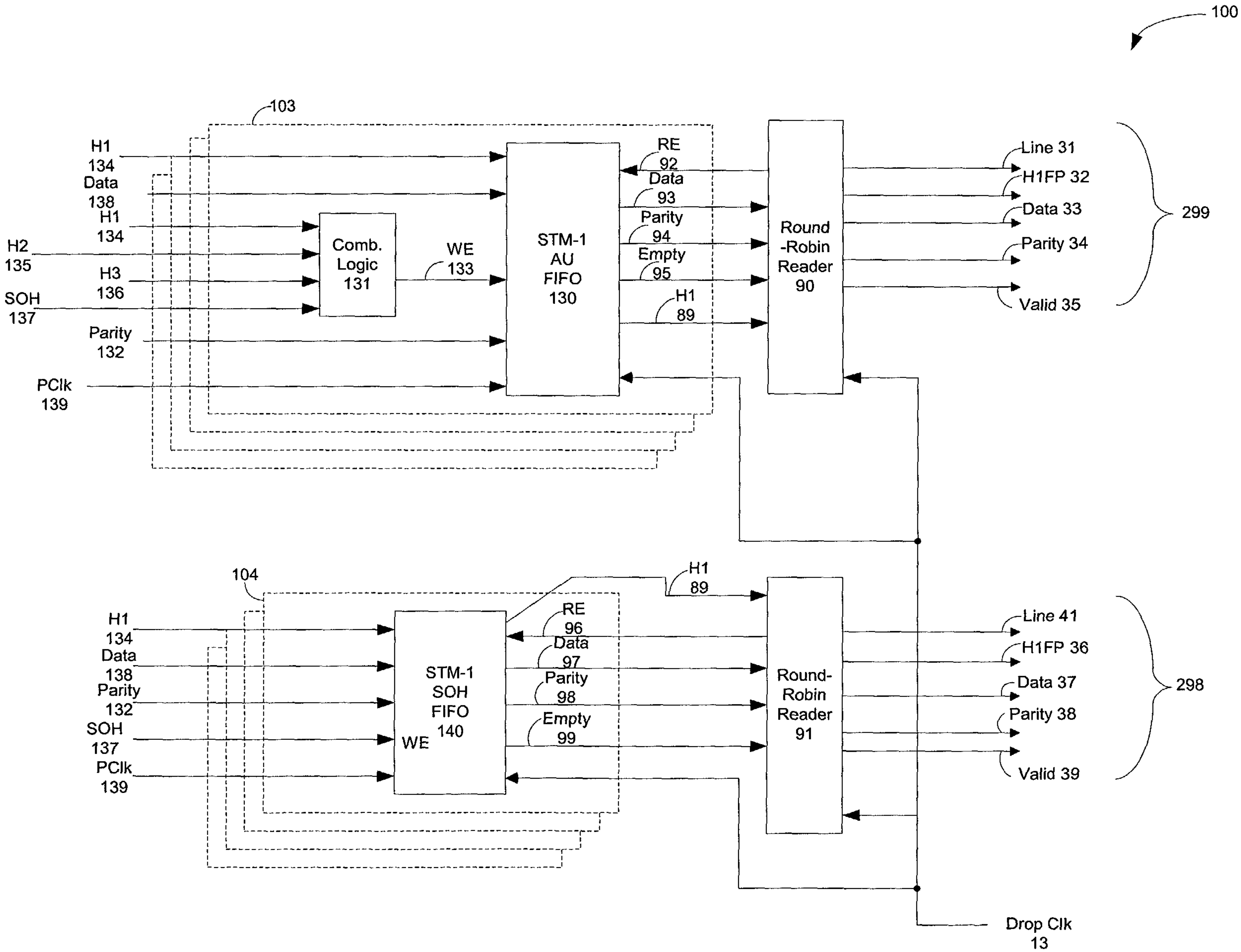
100
103
H1
134
Data
138
H1
134
H2
135
H3
136
SOH
137
Parity
132
PClk
139
Comb.
Logic
131
WE
133
STM-1
AU
FIFO
130
RE
92
Data
93
Parity
94
Empty
95
H1
89
Round
-Robin
Reader
90
Line 31
H1FP 32
Data 33
Parity 34
Valid 35
299
104
H1
134
Data
138
Parity
132
SOH
137
PClk
139
STM-1
SOH
FIFO
140
WE
RE
96
Data
97
Parity
98
Empty
99
H1
89
Round-
Robin
Reader
91
Line 41
H1FP 36
Data 37
Parity 38
Valid 39
298
Drop Clk
13

Figure 2A

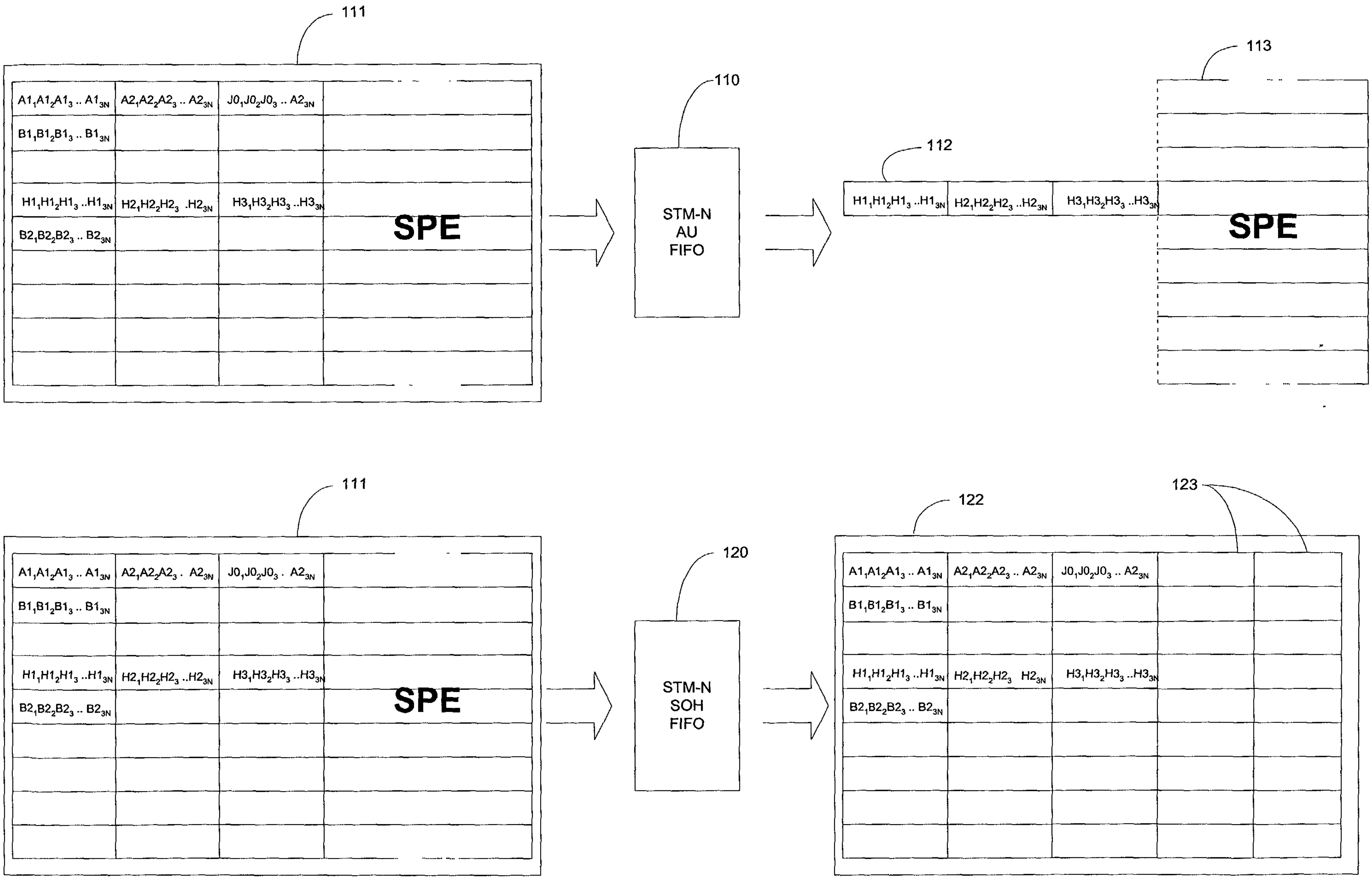
111
$A1_1A1_2A1_3 .. A1_{3N}$
$A2_1A2_2A2_3 .. A2_{3N}$
$J0_1J0_2J0_3 .. A2_{3N}$
$B1_1B1_2B1_3 .. B1_{3N}$
$H1_1H1_2H1_3 ..H1_{3N}$
$H2_1H2_2H2_3 .H2_{3N}$
$H3_1H3_2H3_3 ..H3_{3N}$
$B2_1B2_2B2_3 .. B2_{3N}$
SPE
110
STM-N
AU
FIFO
112
$H1_1H1_2H1_3 ..H1_{3N}$
$H2_1H2_2H2_3 ..H2_{3N}$
$H3_1H3_2H3_3 ..H3_{3N}$
113
SPE
111
SPE
120
STM-N
SOH
FIFO
122
123
$A1_1A1_2A1_3 .. A1_{3N}$
$A2_1A2_2A2_3 .. A2_{3N}$
$J0_1J0_2J0_3 .. A2_{3N}$
$B1_1B1_2B1_3 .. B1_{3N}$
$H1_1H1_2H1_3 ..H1_{3N}$
$H2_1H2_2H2_3$ $H2_{3N}$
$H3_1H3_2H3_3 ..H3_{3N}$
$B2_1B2_2B2_3 .. B2_{3N}$

Figure 2B

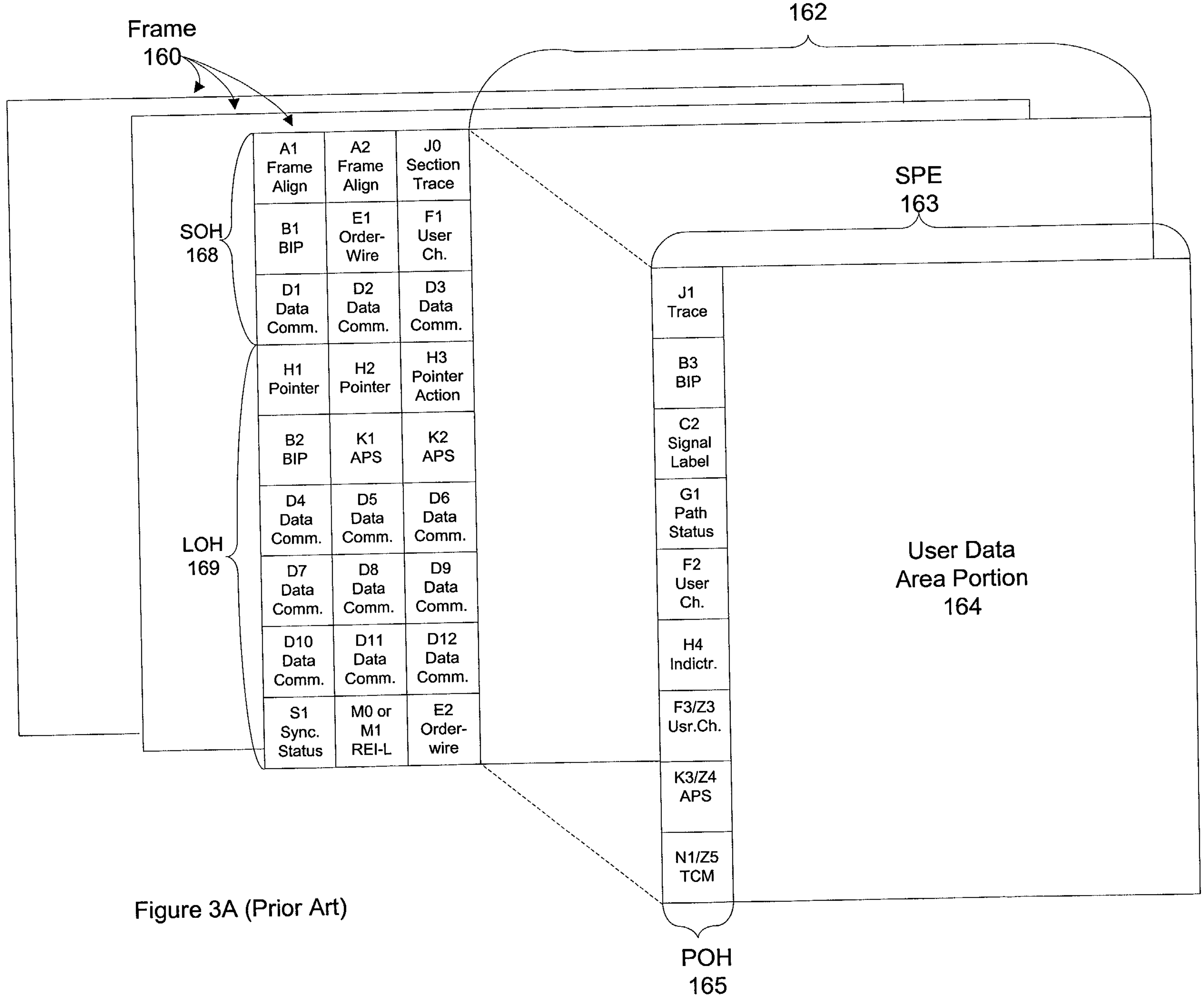

Figure 3A (Prior Art)

Figure 3B (Prior Art)

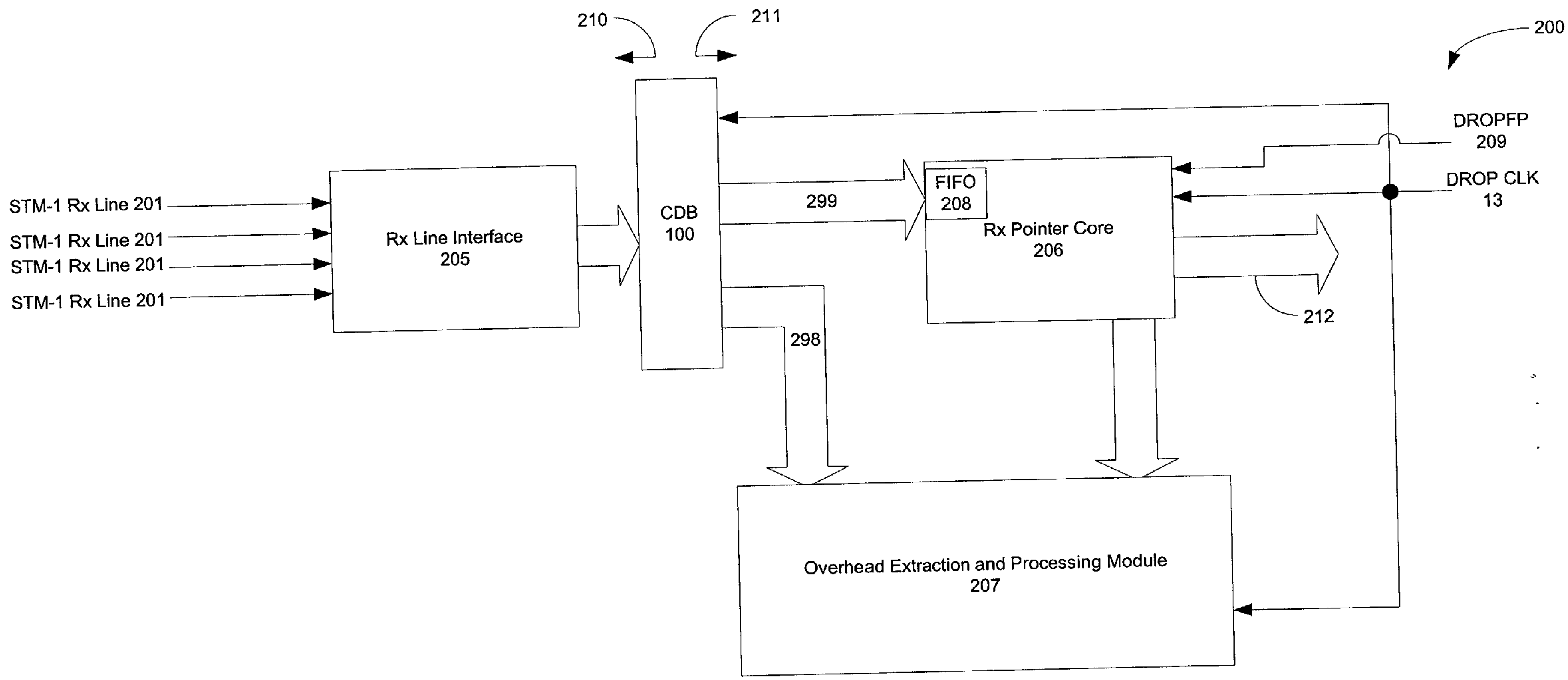
210
211
200
DROPFP
209
DROP CLK
13
STM-1 Rx Line 201
STM-1 Rx Line 201
STM-1 Rx Line 201
STM-1 Rx Line 201
Rx Line Interface
205
CDB
100
299
FIFO
208
Rx Pointer Core
206
212
298
Overhead Extraction and Processing Module
207

Figure 4

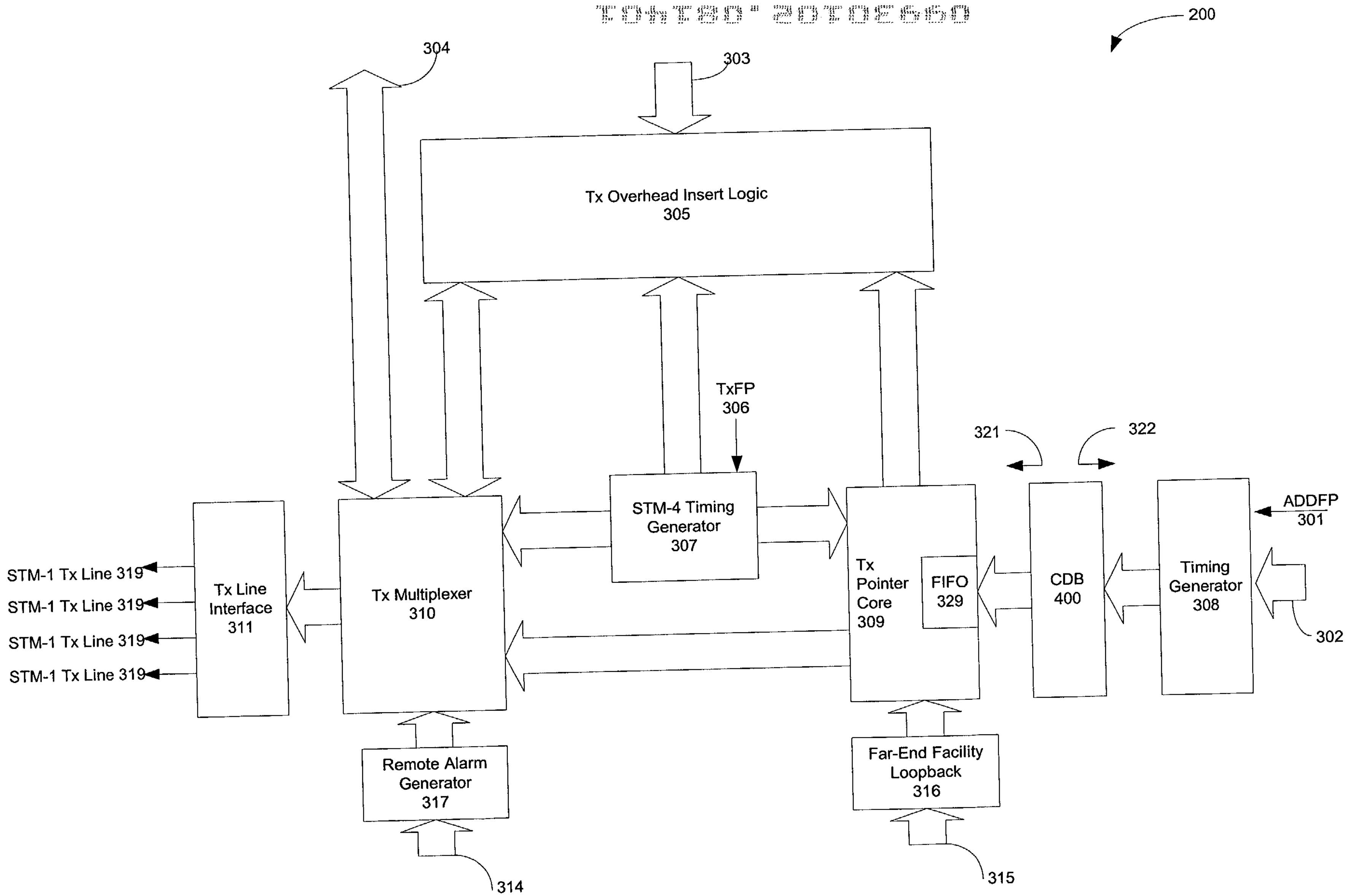

Figure 5

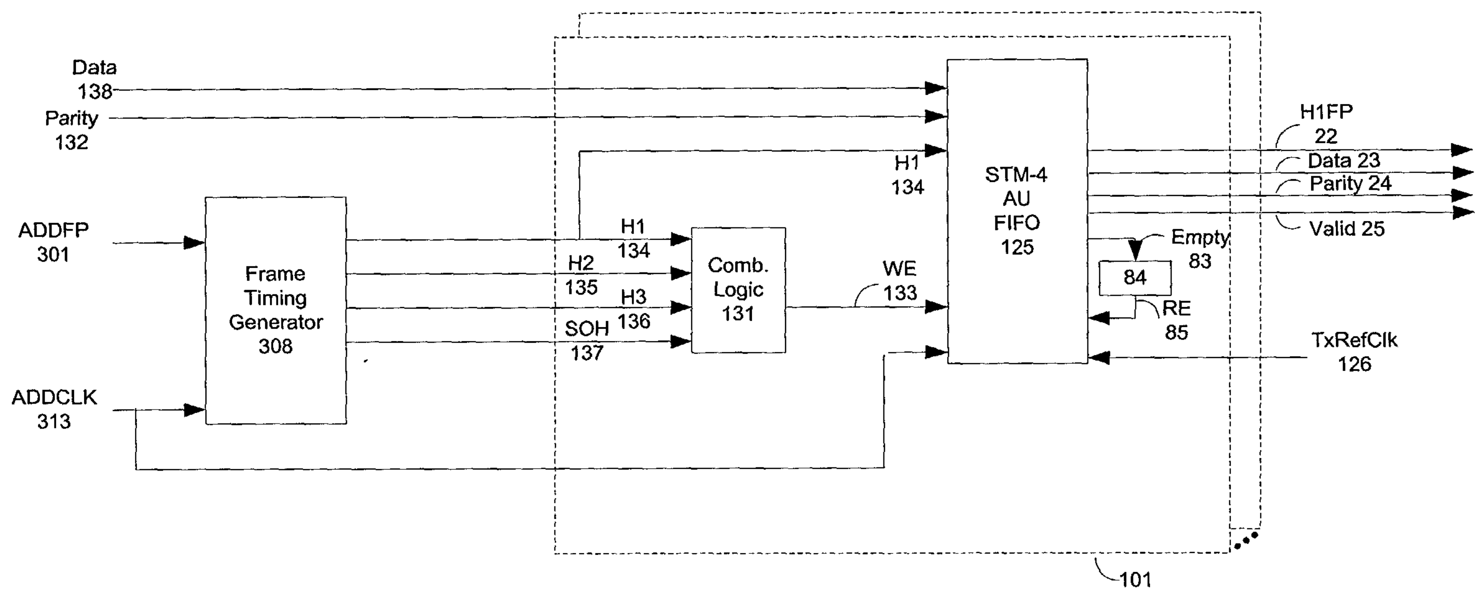
Data
138
Parity
132
ADDFP
301
ADDCLK
313
Frame
Timing
Generator
308
H1
134
H2
135
H3
136
SOH
137
Comb.
Logic
131
H1
134
WE
133
STM-4
AU
FIFO
125
84
Empty
83
RE
85
H1FP
22
Data 23
Parity 24
Valid 25
TxRefClk
126
101

Figure 6

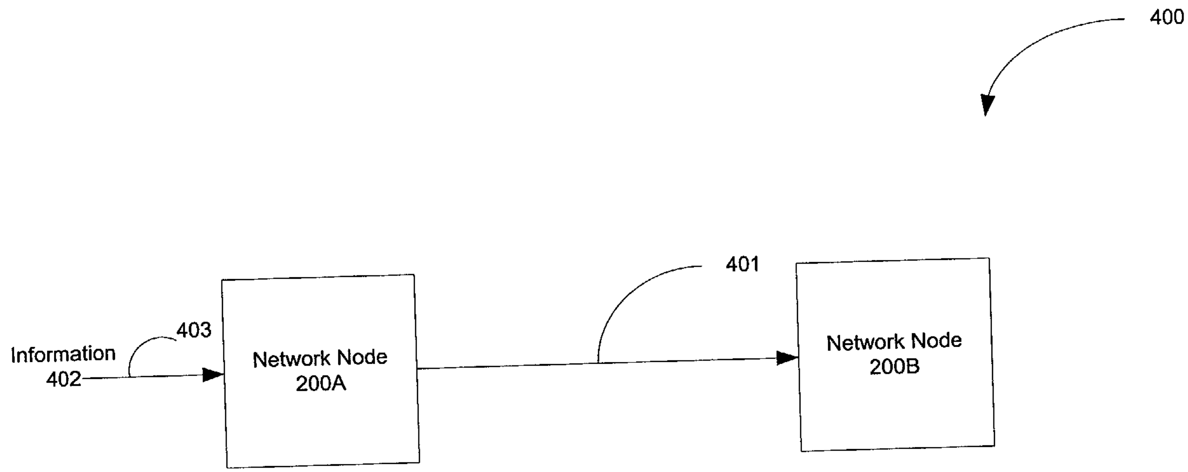
400
401
Information
402
403
Network Node
200A
Network Node
200B

Figure 7